REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1, 3-4, and 6-48 remain in the application. Claims 1, 3, 7, 18-20, and 45 have been amended. Claims 22-44 have been withdrawn. Claims 2 and 5 have been cancelled. Claims 47-48 have been added.

In deference to the requirement in the section entitled "Election/Restrictions" on pages 2-4 of the above-identified Office action, Applicant affirms the election of Group I, claims 1-21 and 45-46 for further consideration.

In deference to the requirement in the section entitled "Claim Objections" on page 4 of the above-identified Office action, appropriate correction of claim 18 has been made.

In the section entitled "Claim Rejections - 35 USC § 112" on pages 4-5 of the above-identified Office action, claims 1, 20, and 45 have been rejected as being indefinite under 35 U.S.C. § 112, second paragraph.

More specifically, the Examiner has stated that "a function of the circuit structure resulting from an interaction of said

layer structures disposed in said etching trenches," "a function of said circuit structure resulting from an interaction of said layer structures disposed in said etching trenches," and "a function of said SRAM memory cells resulting from an interaction of said layer structures disposed in said etching trenches" in claims 1, 20, and 45, respectively, are vague and unclear. These recitations have been deleted.

It is accordingly believed that the claims meet the requirements of 35 U.S.C. § 112, second paragraph. Should the Examiner find any further objectionable items, counsel would appreciate a telephone call during which the matter may be resolved. The above-noted changes to the claims are provided solely for cosmetic and/or clarificatory reasons. The changes are neither provided for overcoming the prior art nor do they narrow the scope of the claims for any reason related to the statutory requirements for a patent.

In the section entitled "Claim Rejections - 35 USC § 102" on pages 5-6 of the above-mentioned Office action, claims 1 and 20 have been rejected as being anticipated by Bryant (US Pat. No. 5,512,517) under 35 U.S.C. § 102(b).

In the section entitled "Claim Rejections - 35 USC § 103" on pages 6-8 of the above-mentioned Office action, claims 2-4,

11, 14-15, 18-19, and 45 have been rejected as being unpatentable Bryant and further in view of Kenney (US Pat. No. 5,744,386) under 35 U.S.C. § 103(a); claim 8 has been rejected as being unpatentable Bryant and Kenney and further in view of Malhi et al. (US Pat. No. 5,225,697) under 35 U.S.C. § 103(a).

The rejections have been noted and claims 1, 20, and 45 have been amended in an effort to even more clearly define the invention of the instant application. More specifically, the feature of claim 5 has been added to claims 1, 20, and 45 respectively. Since claim 5 contains allowable subject matter as indicated by the Examiner in the section entitled "Allowable Subject Matter" on page 9 of the Office action, claims 1, 20, and 45 are now believed to be allowable. Since all of the dependent claims are ultimately dependent on claim 1, they are believed to be patentable as well.

Applicant acknowledges the Examiner's statement in the section entitled "Allowable Subject Matter" on page 9 of the above-mentioned Office action that claims 5-7, 9, 12-13, 16-17, 21, and 46 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The feature of claim 5 has been added to claims 1, 20, and 45 respectively. Since claims 6-7, 9, 12-13, 16-17, 21, and 46 are dependent on allowable claims 1, 20, and 45 respectively, they are believed to be allowable in dependent form.

Claims 47-48 have been added. Claim 47 contains the features of original claims 1 and 10. Claim 48 corresponds to original claim 11.

The Examiner has stated that Bryant in combination with Kenney teaches a SRAM memory cell formed by layer structures disposed in etching trenches. Applicant disagrees. Bryant discloses a silicon substrate including etching trenches disposed at angles with respect to each other and having layer structures. Kenney teaches that layer structures formed in etching trenches may be used in SRAM cells and latches (see column 13, lines 53-54). However, neither Bryant nor Kenney teaches an SRAM memory cell completely formed by a layer structure disposed in etching trenches. The inventive SRAM memory cell layout as recited in claims 47-48 of the instant application results in a reduction of the space requirement in the silicon substrate.

In view of the foregoing, reconsideration and allowance of claims 1, 3-4, 6-21, and 45-48 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made. Please charge any fees which might be due with respect to 37 CFR Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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